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Simulation and Analysis of SRAM Cell Structures at 90nm Technology

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ABSTRACT

SRAM is a most common embedded memory for CMOS ICs and it uses Bistable Latching circuitry to store a bit. This paper represents the simulation of different SRAM cells and their comparative analysis on different parameters such as Power Supply Voltage, Operating Frequency, Temperature and area efficiency etc. All the simulations have been carried out on BSIM 3V3 90nm technology at Tanner EDA tool.

Keywords *– CMOS Logic, Low power, Speed, SRAM and VLSI.*

I. INTRODUCTION

A SRAM cell consist of a latch, therefore the cell data is kept as long as power is turned on and refresh operation is not required for the SRAM cell. SRAM is mainly used for the cache memory in microprocessors, mainframe computers, engineering workstations and memory in hand held devices due to high speed and low power consumption. Each bit in an SRAM is stored on four transistors that form two cross-coupled inverters. This paper compares the different SRAM cells configurations on the basis of the power dissipation, speed, operating frequency range and their temperature dependence with the area efficiency of the circuit.

II. LITERATURE REVIEW OF DIFFERENT SRAM CELLS

2.1 6T SRAM CELL

The schematic diagram of 6T SRAM cell [1] is shown in Fig.1. Access to the cell is enabled by the word line (WL) which controls the two access transistors, in turn, control whether the cell should be connected to the bit lines: BL and BLB. They are used to transfer data for both read and write operations. While it's not strictly necessary to have two bit lines, both the signal and its inverse are typically provided since it improves noise margins.

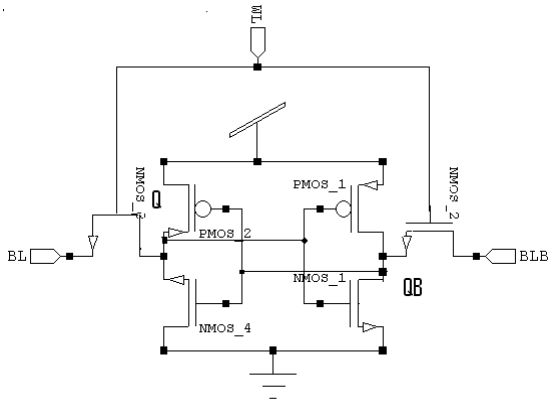

Fig. 1 Schematic of 6T SRAM Cell

2.2 MODIFIED 6T SRAM CELL

Fig. 2 is depicting the circuit diagram of modified 6T [2], [3], [4], [5], [6] SRAM Cell. The transistors NMOS_3, PMOS_4 and NMOS_2, PMOS_1 form cross coupled inverters. Reduction of leakage power is the effective stacking of transistors in the path from supply voltage to ground. This is based on the observation that "a state with more than one transistor OFF in a path from supply voltage to ground is far less leaky than a State with only one transistor OFF in any supply to ground path."

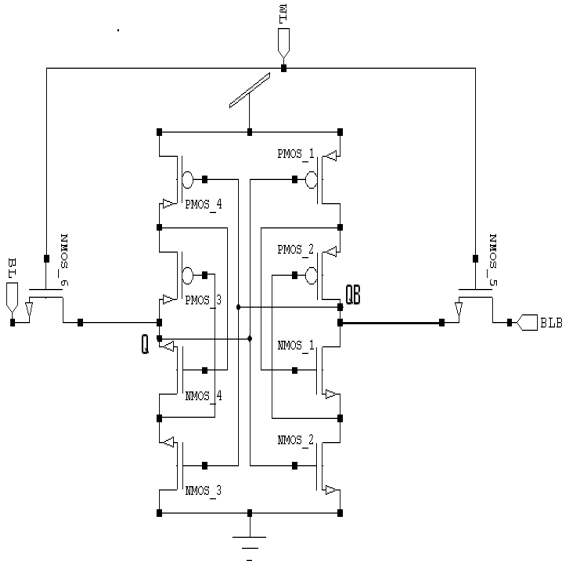

Fig. 2 Schematic of Modified 6T SRAM Cell

2.3 7T SRAM CELL

The 7TSRAM cell [6], [7], [8] uses a novel write mechanism shown in Fig.3. Write mechanism depends only on one of the 2 bit-lines to perform a write operation, which reduces the activity factor of discharging the bit-line pair. The limitation was that area overhead from the conventional 6T SRAM cell

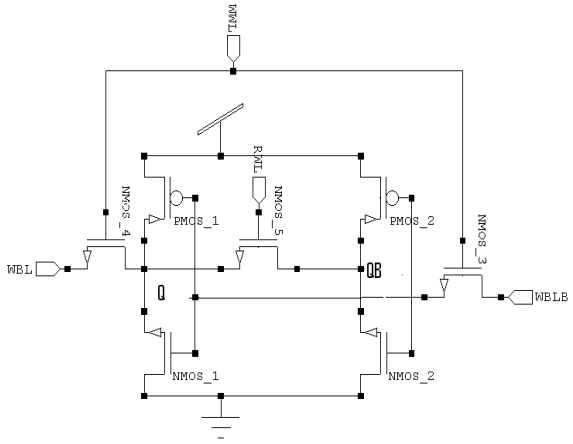

Fig. 3 Schematic of 7T SRAM Cell

2.4 8T SRAM CELL

A dual-port cell (8T-cell) [9], [10], [11] is created by adding two data output transistors to 6T-cell, as shown in Fig. 4. Separation of data retention element and data output element means that there will be no correlation between the read SNM Cell and I Cell. This 8T-cell has 30% more area than a conventional 6T-cell.The 30% area overhead is composed of not only the two added transistors but also of the contact area of the WWL, the word-line for write operations.

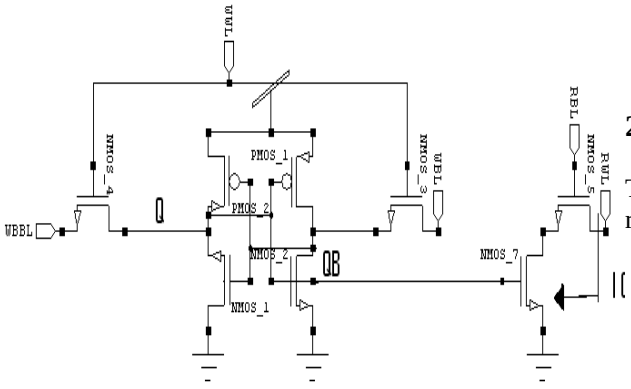

Fig. 4 Schematic of 8T SRAM Cell

2.5 9TSRAM CELL

Schematic of 9T SRAM cell [12] is shown in the Fig. 5. This circuit shows reduced leakage power and enhanced data stability. The 9T SRAM cell completely isolates the data from the bit lines during a read operation. The idle 9T SRAM cells are placed into a super cutoff sleep mode, thereby reducing the leakage power consumption as compared to the standard 6T SRAM cells.

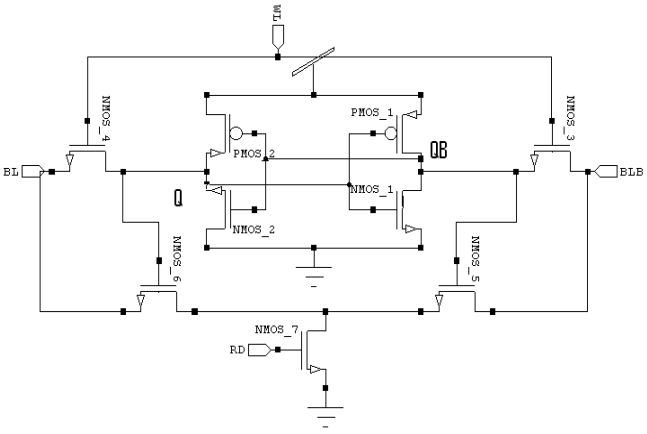

Fig. 5 Schematic of 9T SRAM Cell

2.6 10T SRAM CELL

The dual Port SRAM (10T) [13], [14] as shown in the Fig. 6 has only one read or write can occur per cycle, able to operate the SRAM in Subthreshold region also. The following circuit shows substantial power saving over a low range of power supply voltages.

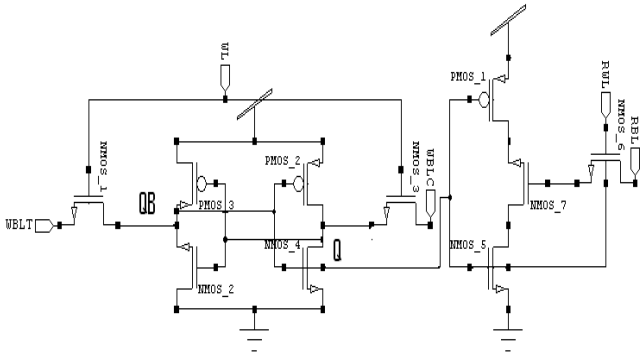

Fig. 6 Schematic of 10T SRAM Cell

2.7 MODIFIED 10T SRAM CELL

Modified 10T SRAM cell [15] is as shown in Fig.7 This circuit shows 10T SRAM Cell with differential read bitlines (BL and BLB).

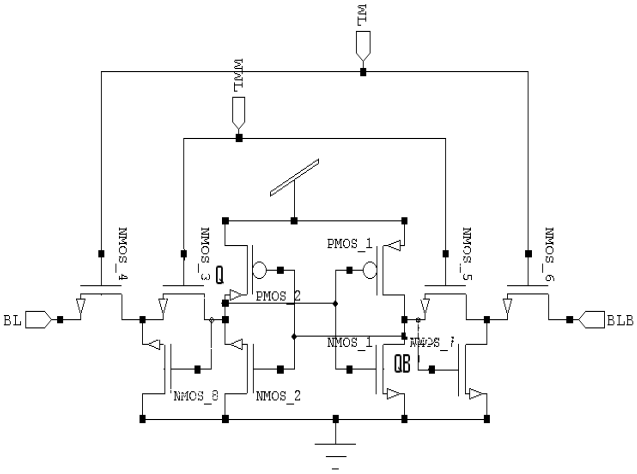

Fig. 7 Schematic of Modified 10T SRAM Cell

Two NMOS transistors (NMOS_4 and NMOS_8) for the RBL and the other additional NMOS transistors (NMOS_6 and NMOS_7) for BLB are appended to the 6T SRAM. As well as the 8T SRAM, precharge circuits must be implemented on the BL and BLB.

2.8 11T SRAM CELL

In Fig. 8 the schematic of the 11T-SRAM cell [16] is shown. Transistors PMOS_3, PMOS_1, NMOS_7, and NMOS_8 are identical to 6T SRAM, but two transistors NMOS_1 and NMOS_2 are downsized to the same size as the PMOS transistors. Minimum size transistors were used for the added 5Tcircuitry, except the access transistor that has a larger size. The most important part of the 11T-SRAM is a boost capacitor (CB) that connects source of NMOS_3 to RDWL.

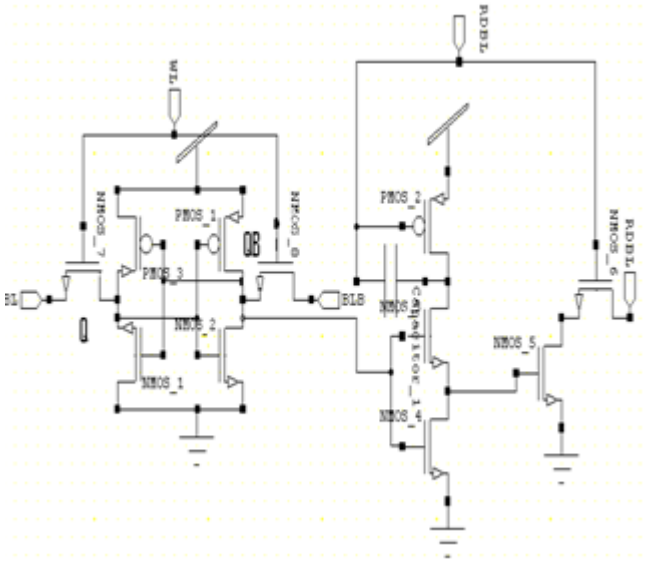

Fig. 8 Schematic of Modified 11T SRAM Cell

III. SIMULATION AND ANALYSIS

3.1 SIMULATION ENVIRONMENT

All the circuits have been simulated using BSIM 3V3 90 nm technology on Tanner EDA tool. To make the impartial testing environment all the circuits has been simulated on the same input patterns. All the simulations has been done on room temperature.

3.2 SIMULATION ANALYSIS

Fig. 9 is depicting the power consumption Vs Vdd for different SRAM cells. Modified 10T SRAM Cell shows the least power consumption over other approaches. Fig. 10 shows delay Vs Vdd for different SRAM cells. The 6T SRAM cell shows least delay among all the other design techniques. The reason for showing maximum speed is the least transistor count in the design approach. Fig. 11 and Fig. 12 shows Power Consumption Vs Operating Frequency and Temperature respectively. Both the above figures depicts shows 10 T Modified SRAM Cell shows always best performance for the range of operating frequency and Temperature among all the other design approaches for SRAM Cell.

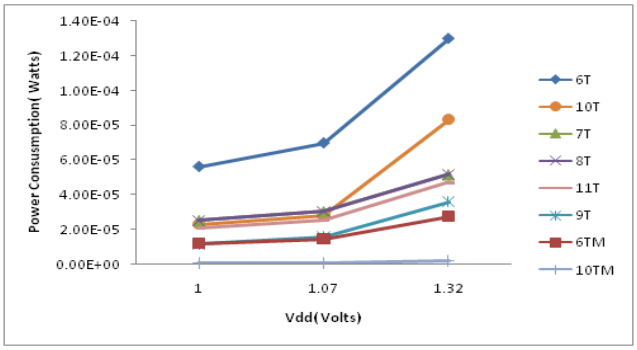

Fig. 9 Power Consumption Vs Vdd for Different SRAM Cells.

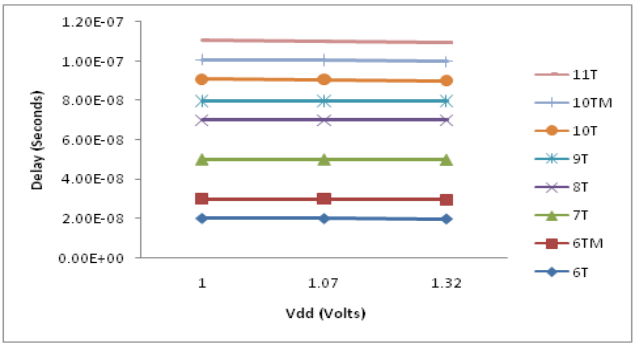

Fig. 10 Delay Vs Vdd for Different SRAM Cells.

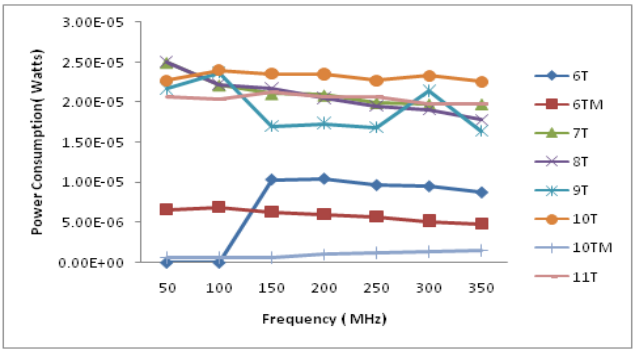

Fig. 11 Power Consumption Vs Operating Frequency for Different SRAM Cells

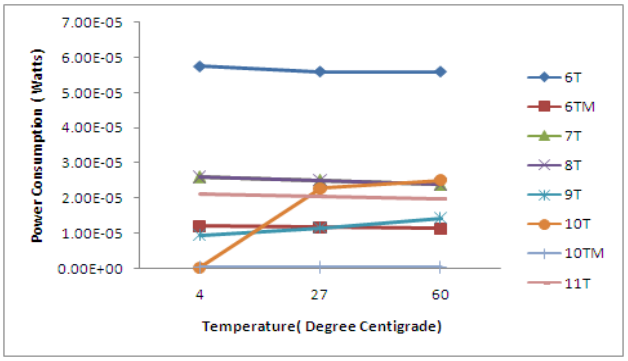

Fig. 12 Power Consumption Vs Operating Temperature for Different SRAM Cells

TABLE 1: Power Delay Product Comparison of Different SRAM Cells

Different SRAM Cells	Power Delay Product (Watt Seconds)		
	Vdd = 1v	Vdd= 1.07v	Vdd=1.32 v
6T	1.12E-12	1.39E-12	2.57E-12
6TM	1.18E-13	1.45E-13	2.69E-13
7T	5.03E-13	6.06E-13	1.05E-12
8T	5.03E-13	6.06E-13	1.05E-12
9T	1.16E-13	1.56E-13	3.49E-13
10T	2.46E-13	3.00E-13	8.60E-13
10TM	**3.04E-15**	**4.85E-15**	**1.78E-14**
11T	2.05E-13	2.52E-13	4.59E-13

TABLE 1 depicts the Power Delay Product over a range of Power Supply voltages and as it is shown in the table that 10 T Modified Designing approach for SRAM Cell shows minimum Power Delay Product.

IV. CONCLUSION

As the battery operated devices are in great demand and to increase their reliability, the life time of battery is a prime concerned but this is done at the cost of speed. But in high speed circuits where speed is the major concern like wireless communications these low-leakage SRAM fails. For low-leakage and high-speed circuits concern should be on both the factors speed and power. This paper tries to find out the solution for SRAM memory cells in both the aspects power consumption and speed or we can say that in terms of power delay product. Modified 10T SRAM Cell shows least power consumption over a range of power supply voltage, operating frequency and operating temperature at the expense of 66.66% area overhead with conventional approach. 6T SRAM Cell shows least delay among all the other design techniques but with the significantly higher power consumption over other approaches. Modified 10 T SRAM Cell shows the least power delay product over a range of supply voltages.

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